ABSTRACT OF THE DISCLOSURE

A method and circuit are disclosed for an integrated circuit having one or more memory cells, each memory cell including first and second p-channel transistor and first and second n-channel transistors configured as cross-coupled logic inverters between first and second reference voltage levels during a normal mode of operation. Power control circuitry is coupled to a source terminal of the first p-channel transistor of each memory cell for providing to the first p-channel transistors the first reference voltage level during the normal mode of operation. This causes a first voltage less than the first reference voltage level to appear at the source terminal of the first p-channel transistors during a data corruption mode of operation wherein data stored in the one or more memory cells is corrupted.